1. A charge pump Phase-Locked Loop (PLL) has the following components
   1. Phase Detector or Phase Frequency Detector – compares the phase of two voltage signals, with two output signals, an UP signal and a DOWN signal. UP is set to high when one of the two (as defined in the network, in this case, V1) goes high first. DOWN is set to high when the other voltage (in this case, V2) goes high first. Both signals are reset as soon as both voltages (V1 and V2) are both high.
   2. Charge Pump – Amplifies charge signal using current mirror to either increase or decrease voltage to throw into loop filter
   3. Loop Filter – Produces the control voltage for the voltage controlled oscillator
   4. Voltage Controlled Oscillator – electronic device that creates an oscillation frequency depending on the voltage applied to the device
   5. %n – Phase Noise Reduction
   6. Clock Network – General clock unit that outputs pulse voltage signals
2. Clock Network topologies include
   1. Tree – Tree network is a commonly used structure in ICs. Signals are transmitted from the root to each leaf.
   2. H-Tree – Symmetric, but large delay. Cannot consider different loads. Usually requires manual design.
   3. X-Tree – Tree with link insertion to reduce skew
   4. Grid – independent of clock load, significant wire capacitance, very robust. Laid out in a grid-like fashion
   5. Meshes – Symmetric
   6. Serpentine – Asymmetric, appears to split randomly from truck (as defined by user) to create spines
3. What is delay uncertainty and what causes it?
   1. Delay uncertainty refers to a variation in the delay of a gate or an interconnect due to several reasons such as process variation, fluctuations in the power supply voltage, and operation temperature.
   2. Delay uncertainty is maximum difference between maximum and minimum victim line delay over all possible cases of switching activity on neighboring aggressor lines.
   3. Caused by crosstalk between victim and aggressor switching simultaneously
4. Compared to asynchronous clocking, synchronous clocks include [Given in homework is in brackets]
   1. Throughput: Worst Case Delay [Instead of average case delay]
   2. Power Consumption: High (Transient Peaks) [Instead of low]
   3. Noise and interference: Worse [Worse]
   4. Circuit Area: Clock Distribution [Clock distribution]
   5. Testability: Good [Instead of poor]
   6. Scalability: Poor (clock distribution sensitive to interconnect and device delays) [Instead of good]
   7. Expandability: Poor (requires clock redistribution redesign) [Instead of good]
   8. Technology Dependence: High [High].
5. Name the three different skew scenarios for a sequentially adjacent pair of registers (Ri -> Rf) and explain what they mean.
   1. The primary design goal in clock distribution networks has been to ensure that a clock signal arrives at every register within the entire synchronous system at precisely the same time.
   2. Zero Skew- This clock skew refers to the arrival of the clock tick simultaneously at transmitting and receiving register.
   3. Positive Skew-This clock skew occurs when the transmitting register receives the clock earlier that the receiving register.
   4. Negative Skew- This clock skew occurs when the receiving register gets the clock earlier than the sending register.
6. What is repeater staggering and why is the technique used?
   1. Repeater staggering is when repeaters in adjacent wires are interleaved and placed in the middle of the two repeaters. This technique is used to reduce worse-case delay and crosstalk noise.